a plurality of serially connected delaying means to receive said external system clock signal and delay said external system clock signal by an incremental period of delay;

a plurality of frequency divider means, whereby a first frequency divider means receives said external system clock signal and divides a frequency of said external system clock signal by a dividing factor and each remaining frequency divider means is connected to an output of one of the serially connected delaying means to divide a delayed external system clock signal by said dividing factor providing a plurality of divided external system clock signals;

a plurality of clock synchronization delay means, whereby each clock synchronization delay means is connected to one of the plurality of frequency divider means to synchronized each divided external system clock signal to the external system clock signal; and

a logical combining means to combine the synchronized, divided external system clock signal to form said internal clock signal.

19. (Amended) The synchronous dynamic random access memory of claim 18 wherein said incremental period of delay is equal to a period of one cycle of said external system clock signal.

20. (Amended) The synchronous dynamic random access memory of claim 18 wherein the number of serially connected delaying means is one less than said dividing factor.

21. (Amended) The synchronous dynamic random access memory of claim 18 wherein the number of frequency divider means is equal to the dividing factor.

22. (Amended) The synchronous dynamic random access memory of claim 18 wherein each clock synchronization delay means is a synchronous mirror delay circuit.

23. (Amended) The synchronous dynamic random access memory of claim 22 wherein the synchronous mirror delay circuit is comprising:

a buffer circuit connected to one of the frequency divider means to buffer, amplify and delay one of the delayed and divided external timing signals to create a first timing signal;

a fixed delay circuit connected to the buffer circuit to delay the first timing signal by a circuit delay factor that is a sum of a first delay factor and a second delay factor, whereby said first delay factor is a delay time of the frequency divider means and the buffer circuit;

a forward delay circuit to measure a difference time period that is the circuit delay factor subtracted from the period of the delayed and divided external timing signal;

a mirror delay circuit connected to the forward delay circuit and the buffer circuit to delay the first timing signal by the difference time period to create a second timing signal; and

an internal buffer circuit connected to the mirror delay circuit to amplify, delay the second timing signal to create the internal clock signal whereby a delay time of said internal buffer circuit is the second delay factor.

24. (Amended) The synchronous dynamic random access memory of claim 18 wherein said internal clock signal controls a transfer of digital data to and from said synchronous dynamic random access memory.

25. (Amended) The synchronous dynamic random access memory of claim 18 wherein the dividing factor is two.

26. (Amended) The synchronous dynamic random access memory of claim 18 wherein the internal clock signal is synchronized with the external system clock signal after four periods of said external system clock signal.

27. (Amended) A synchronous dynamic random access memory to retain digital data, comprising:

a clock generator circuit connected between an external system clock distribution circuit and a plurality of banks of arrays of memory cells, an address circuit, a command circuit, a data control circuit, and a data input/output buffer to provide an internal clock signal to synchronize operation of said synchronous dynamic random access memory, whereby certain operations must occur in time with minimal deviation from said an external system clock signal and whereby said clock generator includes at least one clock synchronizer circuit, comprising;

a frequency divider means that receives said external system clock signal and divides its frequency by a dividing factor to form a divided external clock signal;

a plurality of serially connected delaying means, whereby a first delaying means is connected to the frequency divider means to receive the divided external clock signal, and each delaying means delays said delayed external clock signal by an incremental period of delay to form a plurality of delayed and divided external clock signals.;

a plurality of clock synchronization delay means, whereby a first clock synchronization delay means is connected to frequency divider means and each remaining clock

synchronization delay means is connected to one of the plurality of serially connected delaying means to synchronize each delayed and divided external clock signal to the external system clock signal; and

a logical combining means to combine the synchronized, delayed and divided external clock signals to form said internal clock signal.

28. (Amended) The synchronous dynamic random access memory of claim 27 wherein said incremental period of delay is equal to a period of one cycle of said external system clock signal.

29. (Amended) The synchronous dynamic random access memory of claim 27 wherein the number serially connected delaying means is one less than said dividing factor.

30. (Amended) The synchronous dynamic random access memory of claim 27 wherein each clock synchronization delay means is a synchronous mirror delay circuit.

31. (Amended) The synchronous dynamic random access memory of claim 30 wherein the synchronous mirror delay circuit is comprising:

a buffer circuit connected to one of the frequency divider means to buffer, amplify and delay one of the delayed and divided external timing signals to create a first timing signal;

a fixed delay circuit connected to the buffer circuit to delay the first timing signal by a circuit delay factor that is a sum of a first delay factor and a second delay factor, whereby said first delay factor is a delay time of the frequency divider means and the buffer circuit;

a forward delay circuit to measure a difference time period that is the circuit delay factor subtracted from the period of the delayed and divided external timing signal;

a mirror delay circuit connected to the forward delay circuit and the buffer circuit to delay the first timing signal by the difference time period to create each synchronized, delayed and divided external clock signal; and

an internal buffer circuit connected to the logical combining means to amplify and delay the internal clock signal whereby a delay time of said internal buffer circuit and the logical combining means is the second delay factor.

32. (Amended) The synchronous dynamic random access memory of claim 27 said internal clock signal controls a transfer of digital data to and from said synchronous dynamic random access memory.

33. (Amended) The synchronous dynamic random access memory of claim 27 wherein the dividing factor is two.

34. (Amended) The synchronous dynamic random access memory of claim 33 wherein the internal clock signal is synchronized with the external system clock signal after four periods of said external system clock signal.

REMARKS

Examiner Nguyen is thanked for the thorough examination of the subject Patent Application. The Claims have been carefully reviewed and amended, and are considered to be in condition for allowance.

Reconsideration of the rejection under 35 USC §112, second paragraph, of Claims 18-34 as being as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention is requested in light of the following arguments. The Claims 18-34 are amended to establish proper antecedent basis and appropriate claim dependency. As noted by the Examiner, these amendments correct typographical errors and should now be allowable with the amendments.

The applicant acknowledges that Claims 1-17 and 35-46 are allowable.